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# Comparative Study of Optimally Designed DC-DC Converters with SiC and Si Power Devices

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O. Deblecker, Z. De Grève and C. Versèle

Additional information is available at the end of the chapter

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## Abstract

In this chapter, power losses and mass of optimally designed Si- vs. SiC-based isolated DC-DC converters are compared in quantitative terms. To that end, an adapted version of a computer-aided design tool, previously published by the authors, is used. The database of the existing tool was completed with new wide band gap semiconductor devices currently available from manufacturers. The results are presented for two switch-mode power supplies, each constituted of an isolated DC-DC converter, operating at very different power levels: a 100 kW auxiliary railway power supply and a multiple output 33.5 W power supply intended for a space application. The gains in terms of power losses and mass from one technology to the other can advantageously be evaluated thanks to the developed tool.

**Keywords:** Multiobjective optimization, genetic algorithms, DC-DC converters, SiC devices

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## 1. Introduction

The electric energy is one of the most flexible forms of energy available today, which is mainly due to the development of power electronics over the past decades. Nevertheless, a correct design of power electronic converters is not a trivial task: it usually involves the minimization of multiple conflicting objectives such as, *e.g.* (but not restricted to), the power losses and mass, while ensuring the satisfaction of several technological and thermal constraints. In this context, the authors proposed in a previous work [1,2] a computer-aided design (CAD) tool dedicated

to isolated DC-DC converters, based on multiobjective (MO) optimization using genetic algorithms (GAs). A key advantage of that predesign tool is that it does not restrict to one solution. Instead, it proposes to the designer a set of optimal solutions so that he can choose *a posteriori* which solution best fits the application under consideration or which objective function to favor.

Modern DC-DC power converters often belong to the category of switched mode power supplies (SMPS), for their high-energy efficiency (more than 90%) and their ability to ensure galvanic isolation [3]. Moreover, SMPS are employed in a lot of applications, covering a wide power range (from several tens of watts to hundreds of kilowatts) and fed by different voltage levels. For instance, they are more and more used in vehicular applications (traction and auxiliary converters in trains and electric automobile vehicles) as well as in aeronautics and space.

In addition to passive components, such as filter capacitors/inductors and transformers for providing the electrical isolation, SMPS include power transistors continually switching between low dissipative full-on and full-off states. The switching frequency of those semiconductor devices strongly impacts the design of the magnetic components. Indeed, it is well known that a high-switching frequency yields small values of the core cross section and hence smaller inductors or transformers. Knowing that magnetic components can account for more than 50% of the volume and mass of a power converter, one then understands how crucial it is to use semiconductor devices with fast switching speeds. Yet it should be kept in mind that increasing the switching frequency also increases the switching losses, which can lead to abnormally high-junction temperatures and/or heat sink module dimensions [3]. Currently, the power switches (IGBTs and MOSFETs) as well as diodes are based on silicon (Si) technology, and hence, the continuously increasing demand for lightweight power converters forces the engineers to operate the components at switching frequencies close to their intrinsic limits. This maximum value is however seldom reached, as a trade-off between the switching losses and the speed is needed.

It is now well established in the power electronics community that silicon-carbide (SiC) and gallium-nitride (GaN) semiconductor materials show superior properties, enabling potential power device operation at higher voltages, temperatures, and switching speeds than conventional Si technology (see Figure 1). As a result, this gives rise to new perspectives for the design of power converters with enhanced performances [4–7]. Until now, GaN-based power transistors are still restricted to low voltage applications, whereas SiC components are available with higher voltage ratings and therefore higher power capability. Some manufacturing limitations of GaN devices can be found in [8,9]. Note that, recently, the experimental prototype of a hard switched 20 W/50 V RF GaN-based DC-DC converter intended for use in an envelope-tracking power amplification system has been presented, achieving an efficiency up to 91.6% at 50 MHz [10]. Regarding the performances, power devices based on diamond would be, of course, the most interesting, but this option is not economically acceptable today.

Within this framework, the present contribution aims at comparing in quantitative terms power losses and mass of optimally designed Si- vs. SiC-based isolated DC-DC power converters [11]. To that end, an adapted version of the previously mentioned MO optimization

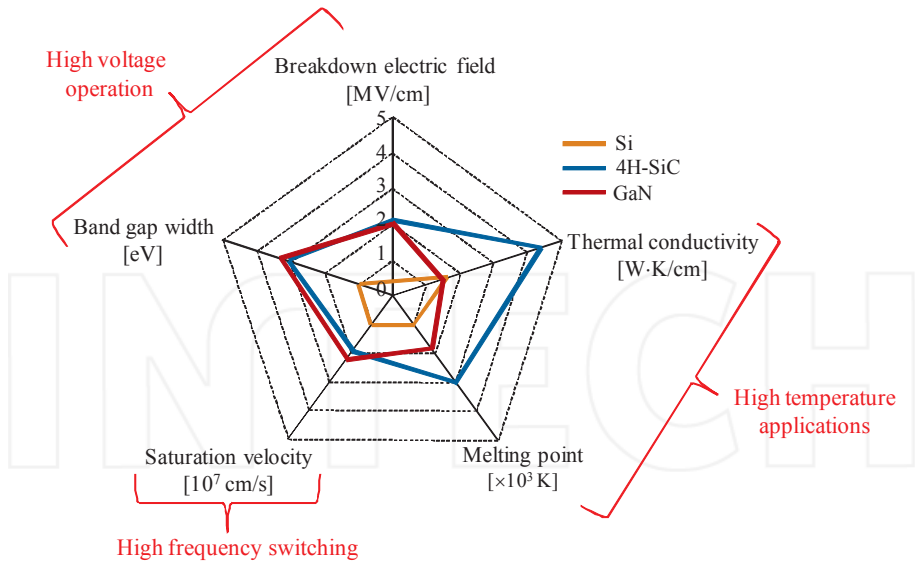


Figure 1. Summary of Si, SiC, and GaN relevant material properties.

CAD tool, completed with a new database of wide band gap semiconductor devices, will be used. Two power supplies operating at very different power levels will be selected as application examples: a high-power (100 kW) auxiliary railway SMPS and a low-power (33.5 W) SMPS intended for a space application.

The remainder of this chapter is organized as follows. In Section 2, a comparison between Si and wide band gap (WBG) materials is first presented. Then the WBG devices (mainly SiC) that will be taken into account in this work are listed in the same section. In Section 3, basic information about the models employed to represent the power converters are given. The existing CAD tool, based on GA, is briefly reviewed in the fourth section. The MO optimal design of the two above-mentioned power supplies, each constituted of an isolated DC-DC converter, is conducted in Sections 5 and 6, with and without including SiC devices in the optimization procedure in order to evaluate the gains in terms of power losses and mass. Finally, conclusions and perspectives are exposed in Section 7.

## 2. Wide band gap materials and power electronic devices

Since the 1950s, WBG materials are expected to replace silicon in semiconductor power devices when it reaches its limits [12]. However, their use in power electronics has been widely considered only recently due to their advantages over Si power devices regarding temperature and power operation [4]. The purpose of this section is to briefly review the intrinsic properties and figures of merit of the principal WBG materials, in comparison with classical Si material.

Then the WBG semiconductor devices (mainly SiC) that will be considered in this chapter are listed.

## 2.1. Properties of wide band gap semiconductors

Several interesting properties of Si and WBG semiconductor materials are reported in Table 1, at a temperature of 300 K [5,13,14]. Note that different polytypes of SiC material exist, each one being characterized by its own crystal lattice structure. They differ in their electronic properties but feature similar mechanical and thermal behavior, which is due to the particular nature of the Si-C chemical link. Among those, the most commonly used is the polytype 4H-SiC.

Properties (at 300 K)	Si	4H-SiC	6H-SiC	3C-SiC	GaN	Diamond
Band gap width $E_g$ [eV]	1.12	3.26	3.03	2.3	3.45	5.45
Breakdown electric field $E_c$ [MV·cm <sup>-1</sup> ]	0.3	2.2	2.5	2	2	10
Intrinsic carrier concentration $n_i$ [cm <sup>-3</sup> ]	$9.6 \times 10^9$	$5 \times 10^9$	$1.6 \times 10^6$	$1.5 \times 10^{-1}$	$1.9 \times 10^{-10}$	$1.6 \times 10^{-27}$
Electrons mobility $\mu_N$ [cm <sup>2</sup> ·V <sup>-1</sup> ·s <sup>-1</sup> ]	1500	1000	500	800	1250	2200
Holes mobility $\mu_P$ [cm <sup>2</sup> ·V <sup>-1</sup> ·s <sup>-1</sup> ]	600	115	101	40	850	850
Thermal conductivity $\lambda$ [W·K cm <sup>-1</sup> ]	1.5	4.9	4.9	3.2	1.3	22
Relative permittivity $\epsilon_r$	11.8	10	9.7	9.7	9	5.5
Saturation velocity $v_{sat}$ [ $\times 10^7$ cm·s <sup>-1</sup> ]	1	2	2	2.5	2.2	2.7
Maximum working temperature $T_{max}$ [°C]	150	760	760	500	800	1100

**Table 1.** Comparison between intrinsic properties of Si and WBG semiconductor materials.

The band gap width  $E_g$  refers to the energy needed for one electron to jump from the valence to the conduction band. A material with a high  $E_g$  implies that the probability for an electron to cross the band gap under thermal excitation is low, thus allowing high working temperature operation. Note that the term “wide band” usually refers to values of  $E_g$  greater than 2 eV [6]. Materials with a high band gap are also less subject to electron jumps caused by radiations, which is an asset in the case of space or nuclear applications.

The maximum working temperature  $T_{\max}$  is defined as the temperature for which the number of intrinsic carriers becomes greater than doping. In that case, the material loses its semiconducting properties. For instance, in Table 1, it can be noticed that WBG materials have higher  $T_{\max}$  than Si. Diamond and SiC are also better heat conductors than Si, according to the values of their thermal conductivity  $\lambda$ .

A WBG also corresponds to a high breakdown electric field  $E_{\sigma}$  which permits to build components with high voltage capabilities (currently up to 20 kV for SiC power devices). Indeed, the breakdown electric field for WBG materials is more or less one order of magnitude higher than for Si, according to the value reported in Table 1. Thus, WBG components might be, for example, interesting candidates for use in power supplies of space traveling wave tubes, which have to produce voltages up to several kilovolts [15].

As explained in [6,14], the reverse leakage current of bipolar junctions is proportional to  $n_i$  or  $n_i^2$ , with  $n_i$  the intrinsic carriers concentration. Thus, considering the values of  $n_i$  in Table 1, the reverse leakage current is several order of magnitudes smaller with WBG components compared to Si.

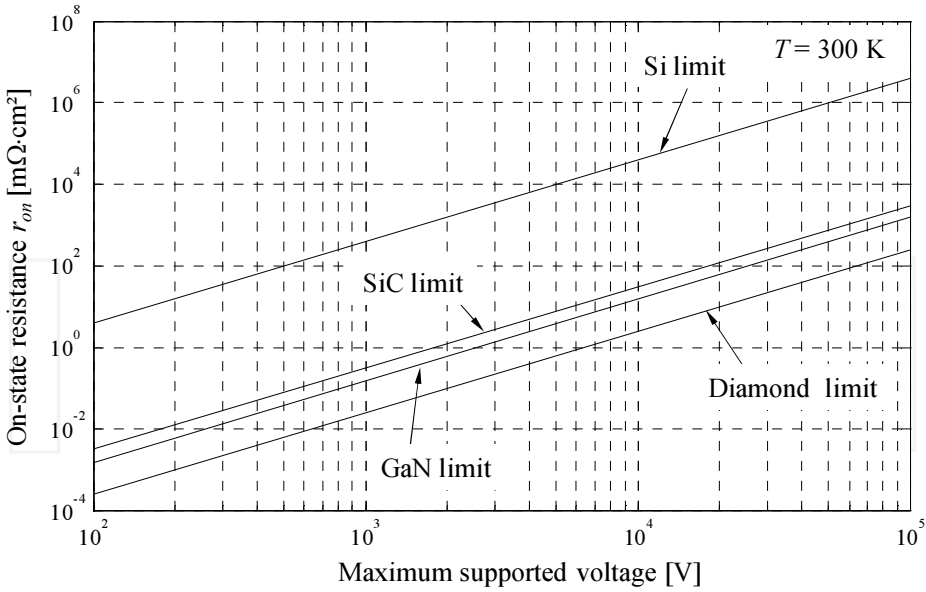
Generally, high values for the charge carrier mobilities  $\mu_N$  (electrons) and  $\mu_P$  (holes), and for the saturation velocity  $v_{\text{sat}}$  (which is the maximum velocity the charge carriers can reach under the application of an electric field), are needed. In that way, it is possible to operate at higher current densities and switching frequencies [16]. It can be seen in Table 1 that SiC and GaN materials have slightly smaller mobilities than Si. Yet that drawback is balanced by a higher saturation velocity. Moreover, a large value of  $v_{\text{sat}}$  combined with small values of the electrical permittivity  $\epsilon_r$  is important for high-frequency applications [14].

The conduction losses essentially depend on  $\epsilon_r$  and the breakdown electrical field  $E_c$ . Indeed, the on-state resistance  $r_{\text{on}}$  of a unipolar component, as, e.g., a metal oxide semiconductor field effect transistor (MOSFET), is inversely proportional to these two variables [14]:

$$r_{\text{on}} \propto \frac{1}{\epsilon_r E_c} \quad (1)$$

This permits to highlight another advantage of WBG components over classical Si ones. Indeed, Figure 2 represents the on-state resistance  $r_{\text{on}}$  as a function of the maximum supported voltage for Si and WBG unipolar components, once again at 300 K. Commonly, a value of a few hundreds of  $\text{m}\Omega \text{cm}^2$  yields reasonable conduction losses. In that case, Figure 2 shows that the maximum supported voltage for Si components is approximately limited to 1 kV, whereas WBG components can support a few tens of kilovolts.

For a comparison of the possible power electronics performances of these materials, some commonly known figures of merit, i.e., special quality criteria, are listed in Table 2 [17,18]. The values reported in this table have been calculated from the data given in Table 1 and normalized with respect to Si. A larger value represents a better material performance in the corresponding category.



**Figure 2.** Theoretical limits of Si and WBG unipolar components on-state resistance as a function of the maximum supported voltage, at 300 K.

Johnson has proposed to use the product of the breakdown electric field and the saturation velocity as a figure of merit (JFM), which determines the ultimate power-frequency capability of the material:  $JFM = (E_c v_{sat} / \pi \tau)^2$ . Later, the following criterion was defined by Keyes:  $KFM = \lambda (v_{sat} / \epsilon_r)^{1/2}$ , which provides a thermal limitation to the switching behavior of transistors. Baliga has proposed yet another figure of merit (BFM) for evaluating a semiconductor material. It is related to the operating losses of a high-power field-effect transistor:  $BFM = \epsilon_r \mu E_c^3$  (with  $\mu$  the mobility of current carriers). However, this criterion was associated primarily with ohmic losses due to the specific on-resistance of the drift region and was used to assess the capabilities of a semiconductor from the standpoint of low-frequency devices. For the assessment of high-frequency devices, the losses associated with the commutations must also be considered. The criterion  $BHFM = \mu E_c^2$ , based on the assumption that switching losses are caused by the recharging input capacitance of a device, was proposed in [18]. Finally, Schneider proposed a figure of merit to assess the performances of high-voltage bipolar components, taking into account the thermal dissipation and maximum operating temperature of the semiconductor material [19]:  $SFM = E_c (\mu_N + \mu_P) \lambda T_{max}$ .

From Table 2, it can be noticed that the figures of merit for diamond are at least 40–50 times more than those of any other semiconductor material (except for Keyes' criterion). On the other hand, SiC polytypes and GaN have more or less similar figures of merit, which implies similar performances.

	Si	SiC (4H)	SiC (6H)	SiC (3C)	GaN	Diamond
JFM	1	215.1	277.8	277.8	215.5	81000
KFM	1	5	5.1	3.7	1.5	35.3
BFM	1	222.8	158.6	129.9	188.3	25319
BHFM	1	35.9	23.1	23.7	37	1629.6
SFM	1	64.4	39.5	19	30.8	5207.1

**Table 2.** Main figures of merit for WBG semiconductors compared with Si.

## 2.2. Wide band gap power devices

Collecting enough information about WBG devices in order to enrich the database of the existing CAD tool was a difficulty of this work. Indeed, these technologies are relatively recent and their market penetration is still at the beginning. Components switching times and losses, on-state resistances, etc., were for instance difficult to obtain. Consequently, an important bibliographical task has been performed in order to create a database sufficiently rich to be exploited, by consulting the scientific literature and manufacturer data sheets, and by participating to international conferences and exhibitions.

Currently, the only SiC semiconductor devices which are widely available are unipolar components (MOSFETs and Junction Field Effect Transistors, or JFETs). On the contrary, bipolar components as, e.g., insulated gate bipolar transistors (IGBTs), are still in research and development phase (some prototypes have nevertheless been presented in literature, see, e.g., [14] for a summary). GaN-on-Si switches have been introduced and commercialized for applications in power electronics converters. These switches benefit from fast switching times of GaN technology while maintaining a comparable cost with Si technology.

Currently, several manufacturers are commercializing WBG power devices. Those that will be considered further in this chapter include the following:

- JFETs available from *SiCED* and *SemiSouth*, with ratings from 500 V/5 A up to 1.2/1.7 kV with current capabilities as high as 52 A. These are normally off components, which means that no source-drain current is needed to keep the polarization between the gate and the source equal to zero.
- SiC MOSFETs currently available from *ROHM Semiconductor* and *Cree*, with ratings from 600 V/10 A up to 1.2 kV/100 A.
- Hybrid modules (Si MOSFET or CoolMOS, with a SiC antiparallel Schottky diode) produced by *Microsemi* (500 V/67 A or 600 V/143 A), which permit to reduce the switching losses compared to classical Si modules [20].
- GaN enhancement mode power transistors (EMPTs) produced by *EPC* with voltage ratings in the range from 40 V to 200 V and current capabilities from 3 A to 33 A.

- SiC Schottky diodes available from *Infineon, Fairchild, Cree, Semisouth, etc.*, with ratings from 600 V/1 A up to 1.2 kV/30 A or 1.7 kV/25 A. Bipolar diodes and Junction Barrier Schottky (JBS) diodes will not be considered in this study.

Note that the database of WBG and classical Si devices will be completed over time in order to extent the design possibilities of the CAD tool. A version of the database is available from [21] but not reported here for the sake of conciseness.

It should also be noted that, even if the maximum working temperature of SiC material is theoretically superior to 700°C (see Table 1), for reasons of packaging, reliability, etc., the components currently available cannot be used at junction temperatures above 200°C (or even 175°C according to some manufacturers) [4]. Likewise, GaN power transistors from *EPC* should not be operated at a junction temperature higher than typically 125°C.

### 3. DC-DC converters modeling

Three types of models are commonly used in the design stages of electrical systems and components, namely, analytical models, simulation models (using dedicated software as, e.g., Saber or PSIM), and finite elements (FE) models. The choice of the type of model results from a trade-off between accuracy and computation time.

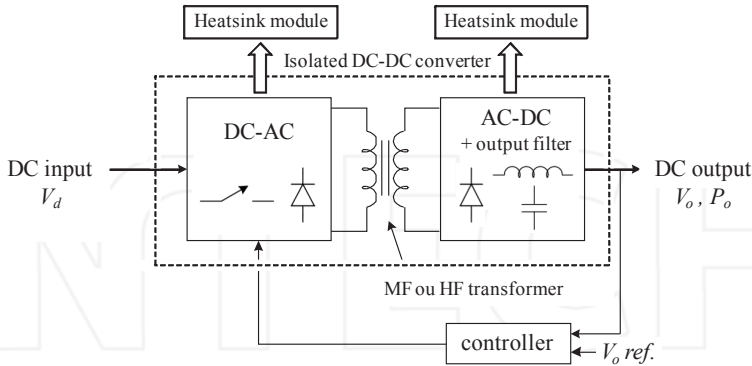
In this contribution, analytical models are adopted mainly for three reasons.

First, most of the analytical models that will be considered are available in the literature and well accepted among the researchers community. Some FE studies have also been conducted to confirm that the analytical and FE models show the same result tendencies. Second, analytical models have a lower computation time compared to the other types of models. This allows for exploring the entire search space in a reasonable amount of execution time when they are included in an optimization procedure. It is a key advantage for this work because the optimization procedure based on GA will require computing the values of the considered objectives a high number of times. Third, even if, in principle, analytical models are less accurate than the other types of models, this should not be taken as a limitation, at least in the scope of this study. Indeed, as the existing CAD tool compares together solutions obtained with the same models, a lack of accuracy in the computation of the objectives will be the same for all the solutions, and so will not affect the final choice of the designer.

The typical structure of an SMPS is shown in Figure 3. A DC input voltage is first converted into AC using a DC-AC (inverter) cell composed of power switches and diodes. A medium- or high-frequency transformer, which often comprises multiple windings, provides the electrical isolation and lowers the voltage levels. The AC voltage is then transformed using an AC-DC (rectifier) cell made of diodes and filtered with passive components (inductors and capacitors). Assuming only one output, the specifications of the converter are given by the three variables  $V_d$ ,  $V_o$ , and  $P_o$ , respectively, the input and output voltages, and the output power. Heat sinks are associated with both cells in order to keep the junction temperatures of



the power devices within acceptable limits. The DC output is typically regulated by means of a feedback control loop that employs a pulse-width modulation controller.



**Figure 3.** Typical structure of an SMPS with an intermediate medium- or high-frequency transformer.

Designing a system using optimization algorithms implies to use models which represent the different constituting parts of the isolated DC-DC converter under study. Indeed, the optimization procedures require multiple evaluations of several objective functions (e.g., the power losses and mass), while satisfying some constraints. Only electric and thermal models are of concern in this work. For the electrical aspect, the following parts need to be modeled:

- *Converter topology.* The flyback, forward, push-pull, half-bridge, and full-bridge topologies are retained as possible candidates for the realization of the DC-DC converter. The steady-state voltage and voltage waveforms are derived by the solution of ordinary differential equations, under some hypotheses [3].
- *Transformer.* The design of the transformer is based on the well-known area product method [22,23]. The transformer power dissipation has also to be estimated since it influences the temperature rise inside the component. The total power losses are divided into two parts: Joule losses in the windings (which are represented by the Dowell model [24] in the case of plain conductors, and by a modified Dowell model for Litz wire [25,26]) and losses in the magnetic core (modeled by a natural Steinmetz equation [27]).
- *Output filter.* The passive components (inductance and capacitance) are designed in order to limit the current and voltage ripples at the converter output [3].
- *Semiconductor power devices.* Conducting and switching losses have to be evaluated for the power devices, as they influence both the junction temperatures and the overall efficiency of the converter. Relevant data, as, e.g., on-state resistance and energies dissipated during the transitions (under given operating conditions), are stored into the database of the tool. In order to allow for a current sharing between the devices, the possibility to associate switches in parallel must also be taken into account.

For the thermal aspect, the following components need also to be modeled:

- *Heat sink modules.* They have to be designed in order to evacuate the heat produced by the conducting and switching losses of the semiconductor power devices, so that it is possible to keep their junction temperatures within acceptable limits. In this work, thermal resistance models are used, combined with information taken from the cooler manufacturer data sheets [28,29]. The heat transfer modes that will be considered further in the application examples are thermal conduction and natural convection (except, of course, for the space application).
- *Transformer.* In practice, the windings and magnetic core temperatures may not exceed the prescribed limits under the risk of being damaged. Thermal resistance networks are used to estimate the working temperatures and hot spots inside the transformer.

Note that all the employed analytical models are described in more detail in [1,21].

#### 4. Existing CAD tool

The existing CAD tool, previously published by the authors [1,2], is briefly reviewed in this section. The basic structure of the tool, founded on a multiobjective optimization using GA, is shown in Figure 4.

The elitist nondominated sorting genetic algorithm, also known as NSGA-II [30], is used to perform search and optimization (such a choice is duly justified in [1,21]), whereas analytic models are used for the modeling of the power converters. The aim of this tool is to design converters optimized with respect to power loss, mass, and cost (the latter objective will not be considered in this chapter), while ensuring the satisfaction of constraints such as, e.g., appropriate limits on transformer or junctions temperature rise. Typical optimization variables (denoted  $x$  in Figure 4) are the switching frequency  $f_s$ , the current density  $J_w$  in the transformer windings, the maximum flux density  $B_m$  in the magnetic core, the transformer size *via* dimensionless coefficients  $k_1$ ,  $k_2$ ,  $k_3$ , the winding conductor diameter  $d_w$ , the core material (among FeSi alloys, ferrite, nanocrystalline material and amorphous material), the conducting material (among copper -Cu- and aluminum -Al-), the type of DC-DC converter topology (among those mentioned in the previous section), the type of semiconductor devices (among silicon-based IGBT and power MOSFET), and the number of these devices associated in parallel per switch  $N_{dev}$ , the number of DC-DC converter cells of the same topology which are associated in serial or parallel  $N_{cell}$  as well as the kinds of input and output connections (series or parallel) of these cells (see Figure 5 for  $N_{cell} = 2$ ).

First, a random initial population is generated. The objective functions  $F(x)$  and constraints  $g(x)$  are evaluated based on the initial population and the specified analytical models of the isolated DC-DC converter. A convergence test is then performed to check for a termination criterion. If this criterion is not satisfied, the reproduction procedure using genetic operators (crossover and mutation) starts. A new population is so generated, and the previous steps are repeated until the termination criterion is verified. Otherwise, the Pareto front, i.e., the

nondominated solutions within the entire search space, is plotted and the optimization procedure ends.

The DC-DC converter modeling part, from which the objective functions are evaluated, is now briefly described. First, the DC-DC converter specifications (input and output voltages, output power, etc.) and the constraints are fed into the computer memory. Then based on the values of some of the optimization variables, the converter topology and the kinds of core and conductor materials are selected. Recall that the design equations of each converter topology and the specifications of the materials are prestored in the computer memory. Once the topology has been chosen, the stresses on the semiconductor power devices and the specifications of the filters and the transformer can be determined. Thus, the semiconductor devices with suitable ratings can be selected from the tool database, and the transformer and filters are designed. Hence, the total power loss of the magnetic components and the semiconductor devices is easily computed by using well-known formulae [31]. Then the heat sink is designed to keep the junction temperature rise of the semiconductor devices within the appropriate limits (typically 125°C for conventional Si-based components).

Finally, it should be noted that the main limitation of the CAD tool here described is that it can only be used in the first stages of the design procedure. In order to use it in the next phases, more accurate models of the converters should be considered.

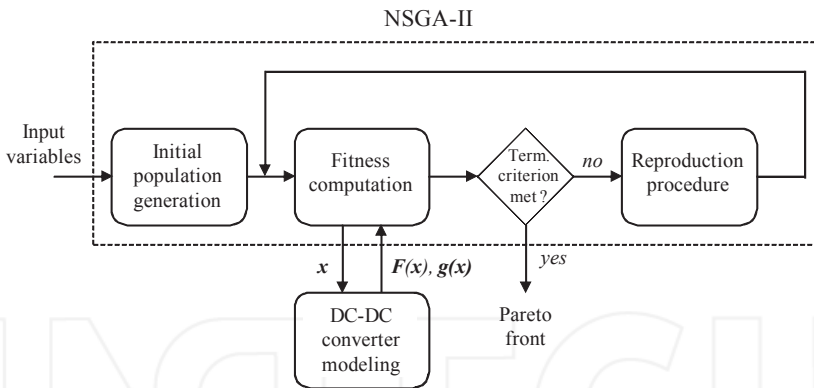


Figure 4. Basic structure of the CAD tool founded on multiobjective optimization using NSGA-II.

## 5. Design of a high-power DC-DC converter for auxiliary railway power supply

### 5.1. Specifications

Auxiliary power supplies are used in modern railways coaches to provide a continuous energy supply to auxiliary equipments such as lighting, air conditioning, pressure protection, etc.

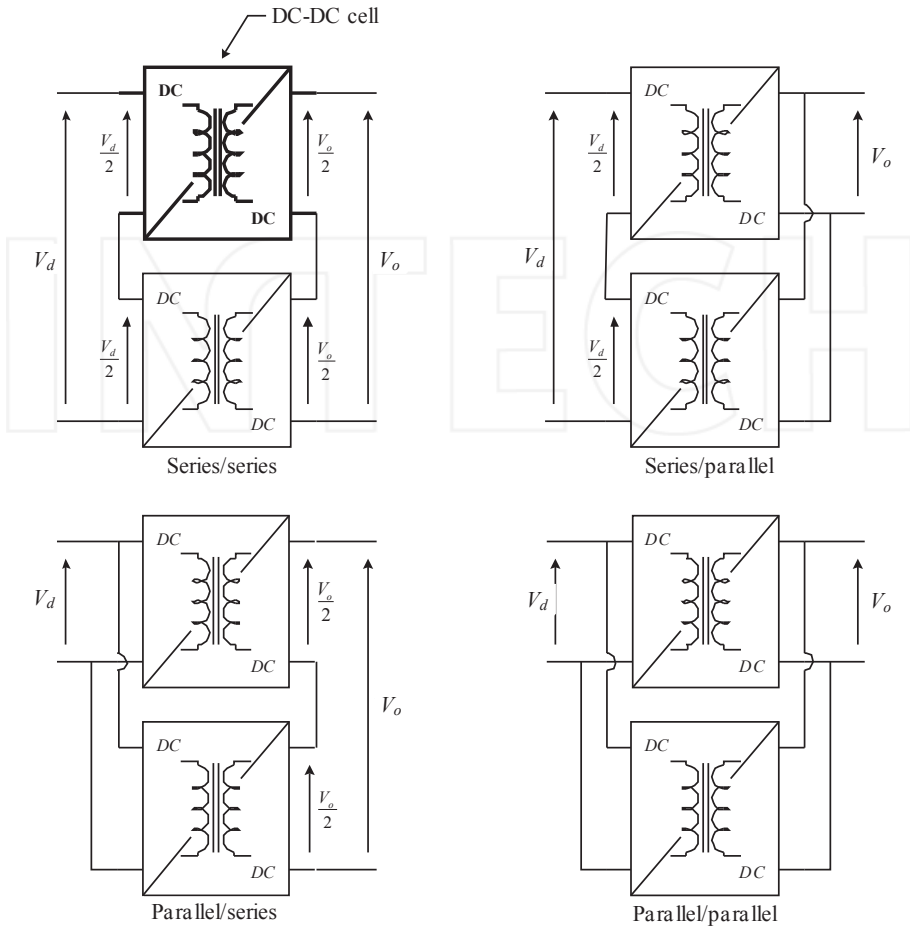


Figure 5. Possible associations between the DC-DC converters cells for  $N_{cell} = 2$ .

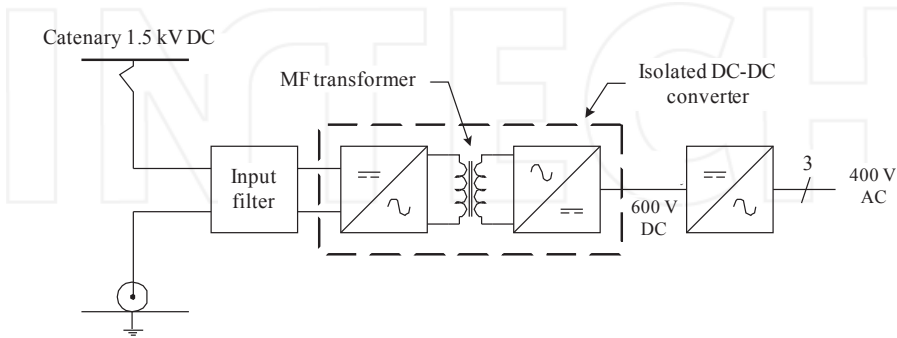
They are directly connected to the catenary and represent the interface between the overhead line and the vehicle onboard low voltage consumers. Currently, the galvanic isolation is realized by a heavy and bulky 50 Hz transformer. However, in order to reduce the size and mass of the devices (filters, transformer, etc.), the trend is to use new structures, which include an intermediate conversion stage using a lightweight MF transformer (typically several kilohertz) [32]. The principle scheme of such a structure to supply a three-phase 400 V AC consumer is illustrated in Figure 6. Note that only the part framed by the dashed line, which represents an SMPS of the type shown in Figure 3, will be subject to the MO optimization.

Some typical electrical specifications of an auxiliary railway SMPS are given in Table 3. These specifications match with a 1.5 kV DC catenary system. The continuous failure-free

operation of the power supply must be guaranteed within the following limits of the DC supply voltage [33]:

$$0.67 V_{d,nom} \leq V_d \leq 1.3 V_{d,nom} \tag{2}$$

where  $V_{d,nom}$  is the conventional nominal value of the catenary voltage.



**Figure 6.** Principle scheme of a high-power SMPS with an intermediate isolated DC-DC conversion stage.

Minimum input voltage	$V_{d,min}$	1 kV
Maximum input voltage	$V_{d,max}$	1.95 kV
DC output voltage	$V_o$	600 V
DC output current	$I_o$	167 A
Output power	$P_o$	100 kW

**Table 3.** Typical specifications of an auxiliary railway SMPS matching with a 1.5-kV DC catenary system.

The optimization variables (denoted  $x$  in the previous section) are listed in Table 4. Recall that, in this contribution, the database of the CAD tool was enriched with WBG semiconductor power devices. Hence, the type of switching semiconductor devices can now be selected among Si IGBT, Si MOSFET, Si MOSFET with SiC antiparallel diode, SiC JFET, and SiC MOSFET. The rectifier diodes can be chosen, as for them, between Si or SiC Schottky devices.

The constraints that have to be ensured are of two natures: thermal and technological. The thermal constraints concern the semiconductor devices (maximum junction temperature limited to 150°C using SiC components) and the MF transformer (maximum temperatures for the windings and the magnetic core which cannot exceed 180°C and 125°C, respectively). From the technological aspect, the lower and upper bounds of each component of  $x$  are reported in the third column of Table 4. The current loss factor (defined from the Dowell model) is also

limited to 1.25, and some constraints must be added in order to verify that the windings can be inserted in the window area of the magnetic component.

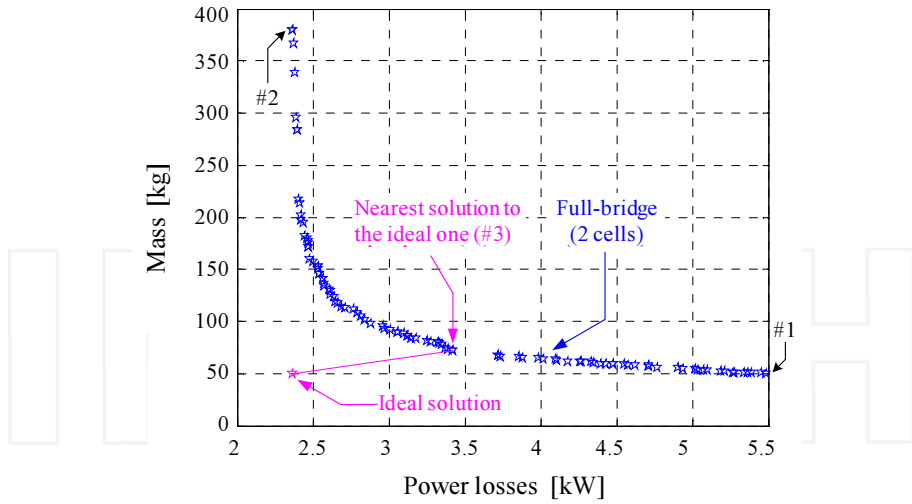
Variables	Type	Bounds (continuous variables)	String length	Possible values (discrete variables)
Switching frequency $f_s$	Continuous	[1; 200] kHz	-	-
Transformer winding current density $J_w$	Continuous	[1; 6] A/mm <sup>2</sup>	-	-
Transformer geometrical factor $k_1$	Continuous	[1; 5]	-	-
Transformer geometrical factor $k_2$	Continuous	[1; 5]	-	-
Transformer geometrical factor $k_3$	Continuous	[1; 2]	-	-
Maximum flux density in magnetic core $B_m$	Continuous	[0.01; $B_{sat}$ ] T	-	-
Winding conductor diameter $d_s$	Continuous	[0.04; 0.56] mm	-	-
Magnetic material	Discrete		2	{0;1;2;3}
DC-DC topology	Discrete		3	{0;1;2;3;4}
Number of parallel semiconductor devices per switch $N_{dev}$	Discrete		2	{1;2;3}
Type of switching semiconductor devices	Discrete		3	{0;1;2;3;4}
Number of DC-DC cells $N_{cell}$	Discrete		2	{1;2;3}
Conducting material	Zero-one		1	{0;1}
Input connection (series or parallel)	Zero-one		1	{0;1}
Output connection (series or parallel)	Zero-one		1	{0;1}
Type of rectifier diodes	Zero-one		1	{0;1}

**Table 4.** Optimization variables for the design of an auxiliary railway SMPS.

## 5.2. Results using SiC and Si technologies

The Pareto front obtained for the two-objective problem (minimizing the power losses and mass) is shown in Figure 7. These results have been obtained in 140 s CPU time, with a 3.4 GHz processor and 3 Gb RAM. The population size, i.e., the number of individuals in the front, and the number of generations were set to 100 and 500, respectively.

All the optimal solutions combine two DC-DC cells in full-bridge topology (series input and parallel output associations). The series input association permits to use semiconductor devices with lower voltage ratings than the maximum input voltage  $V_{d,max}$  (=1.95 kV). The



**Figure 7.** Pareto front of the two-objective problem using SiC and Si devices in the case of the design of a high-power SMPS (blue stars stand for optimal solutions in full-bridge topology).

parallel output association allows for the use of power devices with smaller current capabilities.

For every solution, the number of parallel semiconductor devices (1.2 kV/100 A SiC MOSFET) per switch is two. The rectifier diodes are all Si-based with ratings 1.7 kV/200 A. SiC Schottky diodes are not selected here because, to the best of our knowledge, such current capability is still not available and, in its current state of development, the CAD tool does not offer the possibility to connect several rectifier diodes in parallel.

The values of the other optimization variables are reported in Table 5 for three points of the Pareto front (see solutions 1 to 3 in Figure 7), including solution 3, which is the closest to the ideal one. This utopic solution is constructed by keeping the minimum of each objective separately. As can be seen, some of the variables have converged towards their optimal value. In all cases, the windings are composed of Litz wire (either made of aluminum or copper), with an optimal elementary conductor diameter of 0.2 mm, and the transformer is designed with a ferrite core whose geometrical factor  $k_3$  is approximately 1.6. The maximum flux density  $B_m$  in the core is around 25% of the saturation value  $B_{sat}$  of the employed ferrites. Such a small value results from a trade-off between the two considered objectives, which can be explained as follows.

According to the area product method, which is used here to model the transformer, its mass  $m_{TFO}$  is linked to the maximum flux density by

$$m_{TFO} \propto B_{max}^{3/4} \tag{3}$$

On the other hand, the natural Steimetz equation permits to express the magnetic loss density (in W/kg) as a function of  $B_m$ :

$$P_{\text{magn}} \propto B_{\text{max}}^\beta \quad (4)$$

with  $\beta$  varying between 2 and 2.5, depending on the selected core material. If  $B_m$  is doubled,  $m_{\text{TFO}}$  is multiplied by 0.59 ( $=1/2^{3/4}$ ), whereas  $P_{\text{magn}}$  is multiplied by a value comprised between 4 and 5.65. Hence, the magnetic losses in the core,  $P_{\text{magn}} \times m_{\text{TFO}}$ , are multiplied by a factor between 2.36 and 3.33. Since the mass and the power losses have to be minimized jointly, it can be concluded that the gain in terms of mass with a high value of  $B_m$  does not compensate the ensuing losses. This is the reason of the relatively small values obtained for the maximum flux density  $B_m$  in this design example.

Note that the values of the switching frequency are not discussed here as a detailed analysis will be conducted in the following subsection.

No.	$f_s$ [kHz]	$J_w$ [A/mm <sup>2</sup> ]	$k_1$	$k_2$	$k_3$	$B_m$ [T]	$d_s$ [mm]	Magnetic material	Conducting material
1	22.2	3.27	3.11	3.73	1.61	0.09	0.2	Ferrite	Al
2	10.3	3.22	3.03	3.29	1.61	0.11	0.2	Ferrite	Al
3	4.3	2.32	2.41	2.77	1.59	0.13	0.2	Ferrite	Cu

**Table 5.** Analysis of three solutions of the Pareto front shown in Figure 7.

### 5.3. Comparison with Si technology only

The optimization procedure is now carried out using Si technology only, with approximately the same execution time as above. Hence, the two Pareto fronts using Si and SiC technologies are shown in Figure 8 for comparison.

Using SiC technology clearly leads to lighter power converters with reduced power losses. Let us compare, for example, the power losses at a given mass (say 100 kg). In Figure 8, the corresponding power converters dissipate 4.5 kW in Si technology against only 2.8 kW taking into account SiC devices, which corresponds to a 1.7% gain in terms of efficiency. Similarly, for a given power loss (say 4 kW), the gain in mass is 53% (150 kg in Si technology against 70 kg with SiC).

A detailed analysis of the two Pareto fronts shows that the only design variable which differs significantly from the use of one or the other technology is the switching frequency  $f_s$ . In this vein, Figures 9 and 10 show the variations of the switching frequency along the two Pareto fronts as functions of each objective. As can be seen,  $f_s$  is up to 22 kHz for the optimal solutions designed in SiC, against maximum 6.7 kHz using Si devices only.



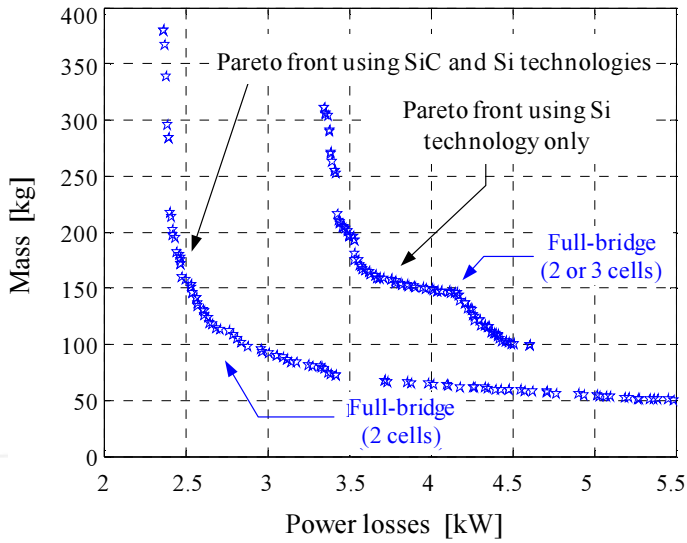


Figure 8. Pareto fronts of the two-objective problem in the case of the design of a high-power SMPS. Comparison between Si only and SiC+Si technologies (blue stars stand for optimal solutions in full bridge topology).

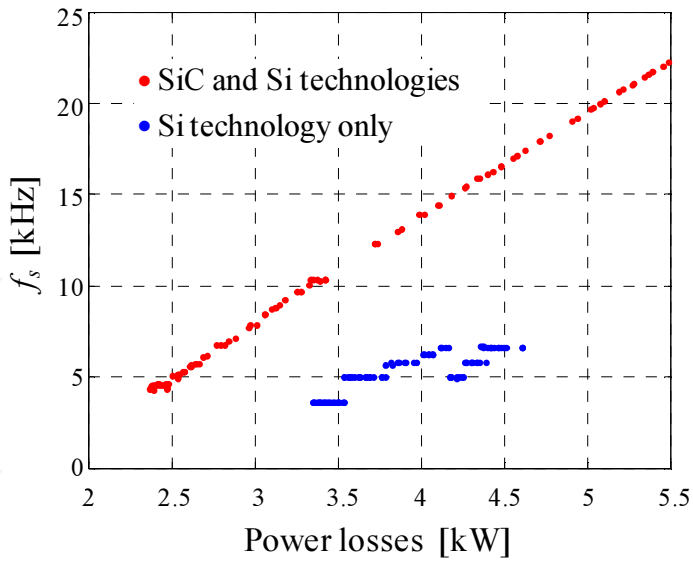
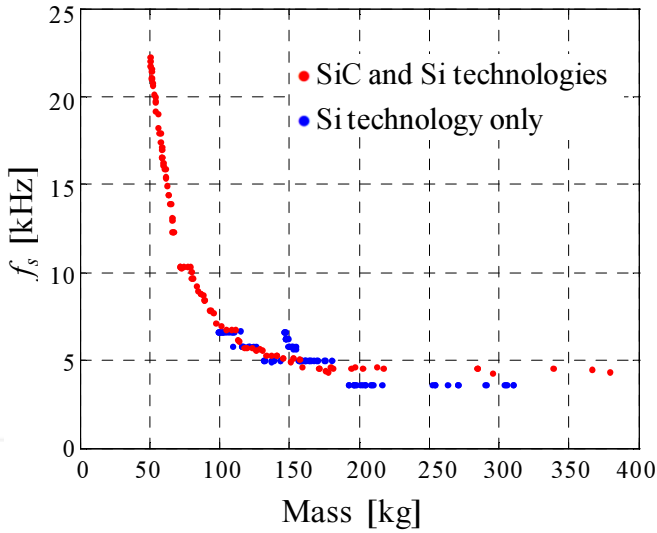


Figure 9. Variation of the switching frequency along the two Pareto fronts shown in Figure 8, as a function of the power losses.



**Figure 10.** Variation of the switching frequency along the two Pareto fronts shown in Figure 8, as a function of the mass.

Several more comments can be made about the results shown in these figures. First, at a given switching frequency, the power losses are significantly reduced in SiC technology. For instance, a reduction of at least 1 kW is expected at 5 kHz, which corresponds to 1 % gain in efficiency. On the other hand, the masses are practically equal at 5 kHz as, for the considered application, the passive components largely contribute to the overall weight. The mass is, however, significantly lowered at higher values of the switching frequency by use of SiC devices.

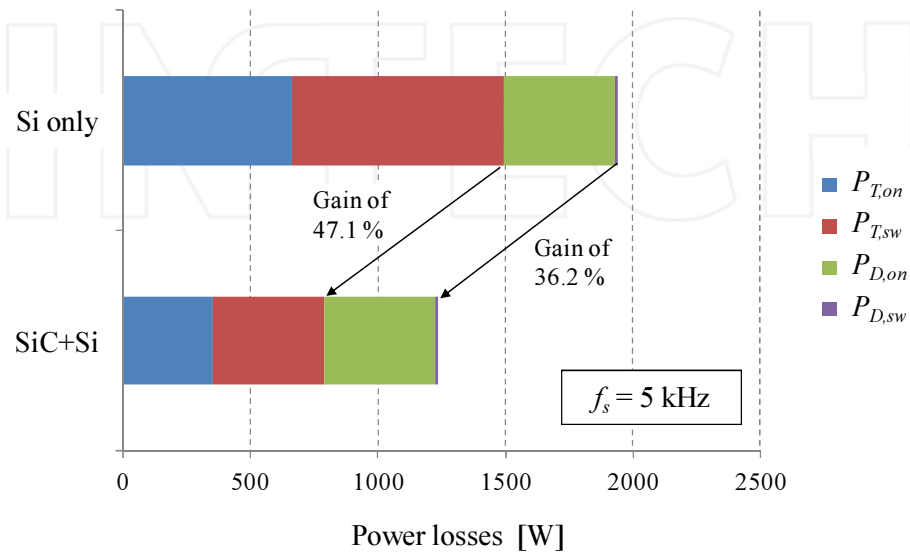
Second, the variation of the switching frequency as a function of the power losses in SiC is more or less linear (see Figure 9), which can be explained by the fact that the total power loss is strongly impacted by the switching losses  $P_{sw}$  proportional to  $f_s$ . On the other hand, the variation of  $f_s$  as a function of the mass can be justified as follows. As said above, the overall mass of the DC-DC converter is mainly dominated by the passive components and, more particularly, the mass of the MF transformer, which is linked to the switching frequency by

$$m_{TFO} \propto f_s^{-3/4} \quad (5)$$

according to the area product method. This result is more or less in line with the shape of the SiC-based evolution represented in Figure 10.

Finally, the power loss distribution (conduction *on* and switching *sw*) related to the devices composing one of the DC-DC cells is shown in Figure 11, considering two solutions of the

Pareto fronts (one on each front in Figure 8) at the same switching frequency of 5 kHz and with the same number of cells. Depending on the technology, the switching devices ( $T$ ) are either 1.2 kV/150 A Si IGBTs or 1.2 kV/100 A SiC MOSFETs. For reasons already mentioned, the rectification stage of the DC-DC cell is made of Si diodes ( $D$ ) with ratings 1.7 kV/200 A, whatever the case. As can be seen in Figure 11, a global power losses reduction of 36.2% is achieved or, even, 47.1% disregarding the losses due the diodes.



**Figure 11.** Power losses distribution in the semiconductor devices of one DC-DC cell of the high-power SMPS. Comparison between Si only and SiC+Si technologies, considering two solutions at the same switching frequency.

## 6. Design of a low-power DC-DC converter for space application

### 6.1. Specifications

Nowadays, SMPS are more and more used in aeronautics and for space applications. Figure 12 shows, for instance, the simplified architecture of a DC power distribution system embedded in a satellite where the primary power source consists of a solar array and batteries. Among all the electronic equipments connected to the main bus, several DC-DC power converters are used for the power matching between the DC interface and the different loads and batteries. These converters are subject to particular constraints related to the space environment that must be taken into account in the early stages of the design procedure. Typical examples of constraints are the presence of ionizing radiation, the absence of convection cooling, the degassing of certain materials, etc [34]. Their reliability is also of prime importance, which

implies *inter alia* that the converters are most often designed fault-tolerant, and that the power switches must be derated with respect to their current and voltage capabilities.

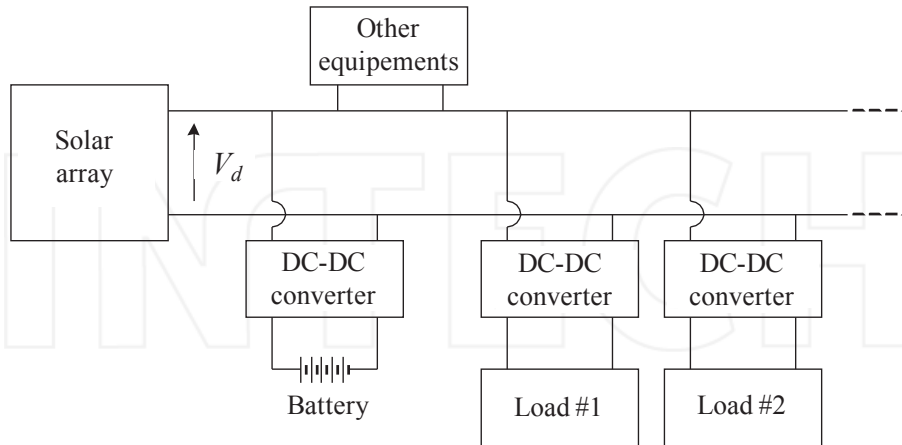
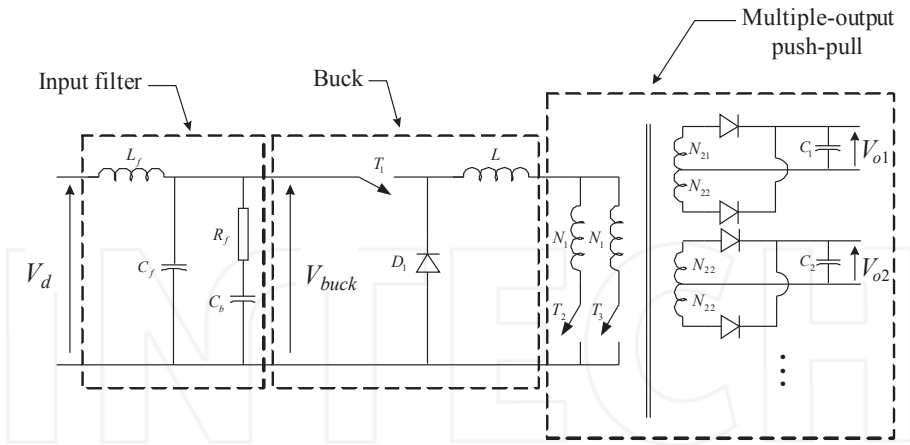


Figure 12. Simplified architecture of a DC power distribution system embedded in a satellite [35].

This section deals with the MO design of an SMPS that can be mounted either on the platform or on the payload side of a satellite (see Figure 13). The power supply has a somewhat more complex structure compared to the previous application example. Indeed, it consists of a cascaded (two stages) DC-DC converter with an input filter [21,36,37]. The front-end stage is used to achieve a step-down (buck) voltage conversion in continuous conduction mode, whereas the back-end stage is a multioutput current-fed converter with a push-pull topology (without output inductor) taken here as an example. The main operational characteristics of the circuit are as follows [37]. First, the switching frequency of the buck stage is twice that of the push-pull converter, which is operating at  $f_s$ . Second, one of the converter outputs (say  $V_{o1}$ ) is controlled by adjusting the duty ratio  $D_B$  of the switch  $T_1$ . Finally, the switches  $T_2$  and  $T_3$  are controlled alternately with a duty ratio of 0.5 (i.e., the push-pull stage just behaves as a non-regulated DC transformer providing electrical isolation). It is important to keep in mind that other topologies can be chosen to realize the output stage as, e.g., a half-bridge or full-bridge converter. It should also be noted that the SMPS considered here is not fault tolerant, in the sense that there is no redundancy of its components, but it tolerates the short circuit of one switch, whatever the stage it belongs to. Even so, in this case, the availability of the power supply will be lost.

The typical electrical specifications of the above shown SMPS are given in Table 6. These are in accordance with the DC-DC converter data sheet available in [36]. The optimization variables  $x$  are reported in Table 7, with their lower and upper bounds. Note that the indices "1" and "2" are chosen to indicate the buck and output stages, respectively. The topology of the latter is considered as an optimization variable. The type of the magnetic core material does



**Figure 13.** Principle scheme of an SMPS intended for a space application (in push-pull topology regarding the back-end stage).

not appear as an optimization variable here because, for the SMPS under consideration, only ferrite cores should be selected from the database due to technological constraints.

Minimum input voltage	$V_{d,min}$	67 V
Maximum input voltage	$V_{d,max}$	102 V
DC output voltage	$V_{o1}$	5 V
	$V_{o2}$	18.3 V
	$V_{o3}$	-18.3 V
	$V_{o4}$	6.15 V
	$V_{o5}$	6.8 V
DC output current	$I_{o1}$	1.9 A
	$I_{o2}$	0.65 A
	$I_{o3}$	0.45 A
	$I_{o4}$	0.3 A
	$I_{o5}$	0.3 A
Output power	$P_o$	33.5 W

**Table 6.** Typical specifications of an SMPS intended for a space application.

Variables	Type	Bounds (continuous variables)	String length	Possible values (discrete variables)
Switching frequency $f_s$	Continuous	[50; 250] kHz	-	-
Inductor winding current density $J_{w,1}$	Continuous	[1; 6] A/mm <sup>2</sup>	-	-
Transformer winding current density $J_{w,2}$	Continuous	[1; 6] A/mm <sup>2</sup>	-	-
Maximum flux density in inductor core $B_{m,1}$	Continuous	[0.01; 0.38] T	-	-
Maximum flux density in transformer core $B_{m,2}$	Continuous	[0.01; 0.38] T	-	-
Inductor wire diameter $d_{s,1}$	Continuous	[0.032; 0.5] mm	-	-
Wire diameter of transformer coil $d_{s,2}$	Continuous	[0.032; 0.5] mm	-	-
DC-DC topology (output stage)	Discrete		2	{0;1;2}
Number of parallel semiconductor devices per switch $N_{dev,1}$	Discrete		2	{1;2;3}
Number of parallel semiconductor devices per switch $N_{dev,2}$	Discrete		2	{1;2;3}
Type of switch $T_1$	Discrete		3	{0;1;2;3;4}
Type of switches (output stage)	Discrete		3	{0;1;2;3;4}
Number of DC-DC cells $N_{cell}$	Discrete		2	{1;2;3}
Conducting material	Zero-one		1	{0;1}
Input connection (series or parallel)	Zero-one		1	{0;1}
Output connection (series or parallel)	Zero-one		1	{0;1}
Type of diode $D_1$	Zero-one		1	{0;1}
Type of rectifier diodes	Zero-one		1	{0;1}

Table 7. Optimization variables for the design of an SMPS intended for a space application.

## 6.2. Changes to the existing tool

In order to address this design problem, it was necessary to adapt the existing CAD tool to the specific requirements of the SMPS for space application. The main changes to the analytical models have been described in detail in [37]. They are briefly reviewed below:

- *Magnetic components.* The magnetic core is now selected from a database of ferrite cores (instead of being optimized from dimensionless geometric coefficients). In the case of a transformer, the RM ferrite core, which has an area product directly superior to the calculated value, is selected from the database. In the case of an inductor, a toroidal core is chosen instead of an RM type one for reasons of mechanical design. Note also that enameled wire is used for windings instead of Litz wire.
- *Derating of the semiconductor devices.* In order to improve the reliability of the power converters used in space environment, different actions must be taken at the early design stage [38]. Among them, a part stress analysis is always performed taking into account the

maximum operating temperature, which results, in particular, in a reduction of the voltage and/or current ratings of the various components. Thus, for this application, a 50% voltage derating of the semiconductor devices is applied. Their current capability is also derated according to the junction temperature value of the component. A 50% current derating is adopted up to a junction temperature of 70°C and, above this limit, the current capability declines linearly to zero at 110°C.

- *Cooling of the components.* As there is no exchange of heat by convection in the vacuum and radiation is negligible inside the satellite, the thermal models must be modified to take into account only the heat transfer by conduction. For this application, the various components are located on a heat-pipe cooled plate, which is assumed isothermal at 60°C. The thermal model of a semiconductor device is represented with two thermal resistances, one between junction and case and the other between case and cooled plate. Similarly, the cooling of a magnetic component is only by conduction through the core surface in contact with the plate (through an aluminum sole-plate). An equivalent circuit of thermal resistances is adopted to deal with the heat transfers between the various parts of the element itself.

Note also that the design of the input filter shown in Figure 13 was fully described in [39], as well as the optimization of its shunt damping circuit. Thus, in the present contribution, this part of the SMPS is not directly optimized by GA. Instead, the procedure to calculate the filter elements was implemented as exposed in [37].

### 6.3. Results using SiC and Si technologies

The Pareto front of the two-objective problem using SiC and Si devices is represented in Figure 14. As can be seen, the power losses are reduced as the proportion of SiC devices grows. The CPU time needed to obtain these results was 173 s, which is comparable to the execution time related to the previous application example (with the same population size and number of generations).

All the optimal solutions are designed with only one DC-DC cell (regarding the output stage), which corresponds to either a full-bridge or a push-pull configuration. The half-bridge topology is not retained here because, in that case, a capacitive divider is needed to obtain a voltage source behavior and the output filter inductor cannot be eliminated, which yields a higher number of passive components. It can be observed in Figure 14 that the full-bridge topology is interesting at low loss, but a higher mass since more semiconductor devices are needed, whereas the push-pull architecture is clearly the best trade-off between both objectives. The rectifier diodes are all Si-based with ratings 100 V/3 A for output 1 and 100 V/1 A for outputs 2 to 5. Indeed, the SiC diodes available from the current CAD tool database are rated at least for 600 V/1 A, which is much too high for the output voltage levels specified in Table 6.

The values of the other optimization variables are reported in Table 8 for six particular solutions, including solution 4, which is the closest to the ideal point. Most of them have converged towards their optimal value. In particular, it is noticed that the switching frequency

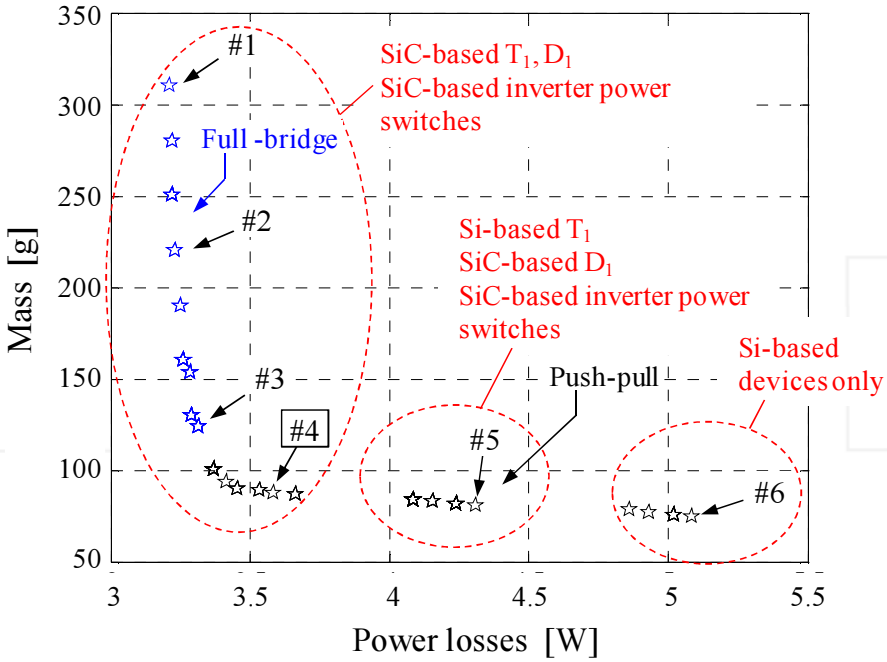


Figure 14. Pareto front of the two-objective problem using SiC and Si devices in the case of the design of a low-power SMPS (blue and black stars stand for optimal solutions in full-bridge and push-pull topologies, respectively).

remains practically unchanged along the Pareto front (but for solution 4 where  $f_s$  is equal to 141 kHz), which is in contrast with the previous design example.

In the power supply, the overall mass is distributed among the passive components (transformer, etc.) and the semiconductor power devices. The corresponding repartition is shown in Figure 15 for the six solutions of interest. Unlike the application of an auxiliary railway SMPS, it can be seen that the passive components are no longer the main contributors with respect to that criterion, and for certain solutions, their mass may even be much less than that of the semiconductor devices (see, e.g., solution 1). This can be justified from the fact that the mass of a ferrite core (say of RM8 type), which has a strong impact on the calculation of the mass linked to the passive components, can be estimated at 13 g, whereas the one of a JFET SiC 500 V/5 A is already about 15 g and several of them are needed to constitute only one switch of the output stage.

In the same way, Figure 16 shows the distribution of the power losses among the passive components and the semiconductor power devices. For the latter, the distinction is made between the conducting and switching losses. It can be observed that the total power dissipation is mainly due to the on-state power losses, whatever the solution. The switching losses are, as for them, growing in importance as the proportion of SiC devices decreases from



No.	$f_s$ [kHz]	$J_{w,1}$ [A/mm <sup>2</sup> ]	$J_{w,2}$ [A/mm <sup>2</sup> ]	$B_{m,1}$ [T]	$B_{m,2}$ [T]	$d_{s,1}$ [mm]	$d_{s,2}$ [mm]	Trans-former core	Conduc-ting material	Diode D <sub>1</sub>	Switch T <sub>1</sub>	Switches (output stage)
1	123	2	3.5	0.37	0.05	0.04	0.33	RM8	Al	SiC 600 V/1 A	V/5 A (6 in parallel)	JFET SiC 500 V/5 A (3 in parallel)
2	123	2	3.5	0.37	0.05	0.041	0.33	RM8	Al	SiC 600 V/1 A	V/5 A (4 in parallel)	JFET SiC 500 V/5 A (2 in parallel)
3	123	2	3.5	0.37	0.11	0.04	0.33	RM8	Al	SiC 600 V/1 A	V/5 A (2 in parallel)	JFET SiC 500 V/5 A
4	141	3.2	3.8	0.38	0.19	0.041	0.33	RM6	Al	SiC 600 V/1 A	V/5 A (2 in parallel)	JFET SiC 500 V/5 A
5	124	3.6	3.8	0.38	0.13	0.04	0.33	RM8	Al	SiC 600 V/1 A	MOSFET Si 500 V/10 A (2 in parallel)	JFET SiC 500 V/5 A
6	124	3.6	3.8	0.38	0.22	0.04	0.33	RM7	Al	Si 150 V/1 A	MOSFET Si 500 V/10 A (2 in parallel)	MOSFET Si 500 V/10 A

**Table 8.** Analysis of six solutions of the Pareto front shown in Figure 14.

solutions 1 to 6, and the power losses in the passive components are about one order of magnitude less than the conduction losses.

#### 6.4. Comparison with Si technology only

For comparison, the two Pareto fronts with and without including the selection of SiC devices in the optimization procedure are shown together in Figure 17. As can be observed, the two Pareto fronts merge each other when the objective of mass is preferred, which is consistent with the results reported in Figure 14 (where the lighter solutions are Si-based only). For a given mass (say 100 g), the power supply dissipates 4.6 W with Si against only 3.4 W, taking into account SiC devices, which corresponds to a 3.6% gain in terms of efficiency. Note also that all the solutions obtained with Si technology only correspond to one DC-DC cell in push-pull topology.

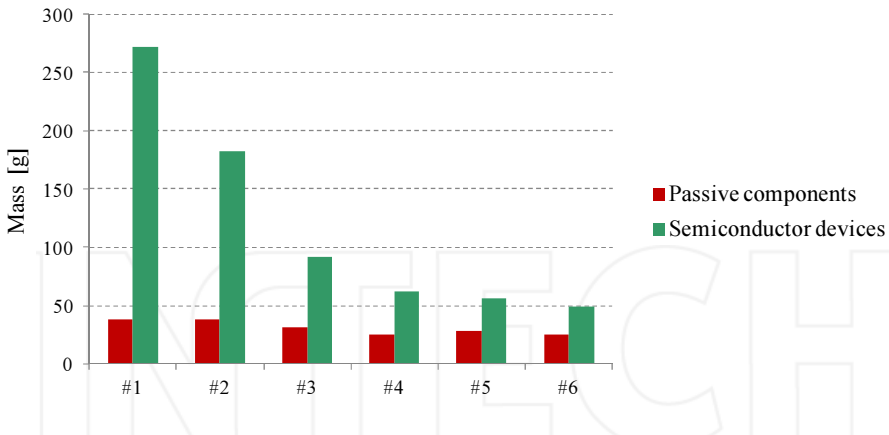


Figure 15. Repartition of the masses between the passive components and the semiconductor power devices for the six particular solutions in Table 8.

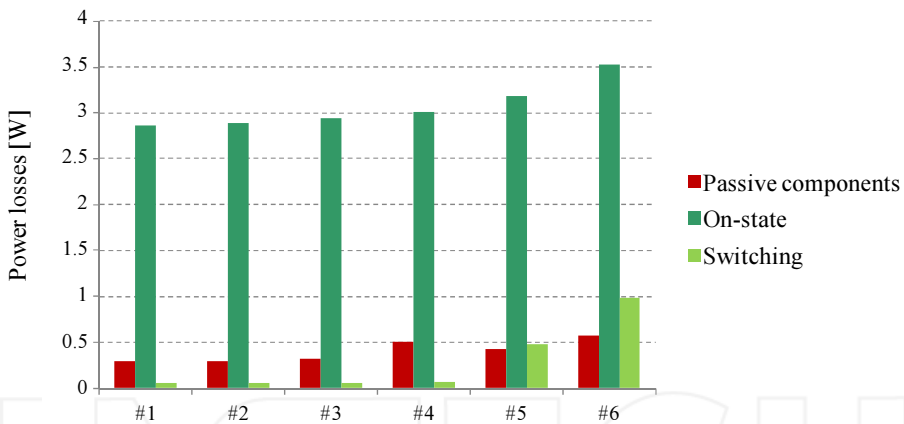
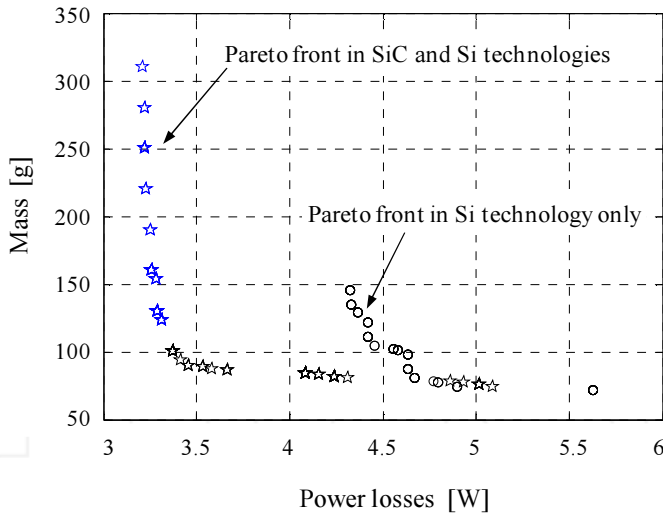


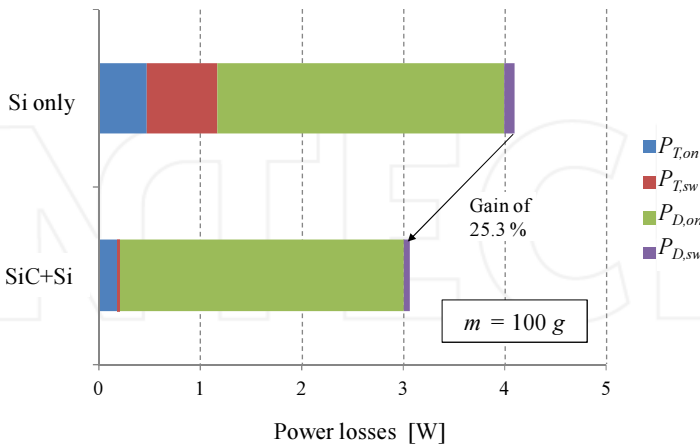
Figure 16. Distribution of the power losses among the passive components and the semiconductor devices (on-state and switching power losses) for the six particular solutions in Table 8.

Finally, Figure 18 compares the power losses in the semiconductor devices, with and without SiC. To that end, two solutions of the Pareto fronts having the same mass of 100 g (one on each front in Figure 17) are selected. The switching frequency is equal to 100.2 kHz for the Si solution and to 119.9 kHz for the SiC one. Globally, a power losses reduction of 25.3% is obtained using SiC JFETs instead of Si MOSFETs as switching devices. As can be observed, the switching losses in the power transistors ( $P_{T,sw}$ ) are more particularly decreased (a gain of 97% is achieved in this case). On the other hand, as above-mentioned, all the rectifier diodes are Si-based, and that even for the solutions designed with SiC components. This is the reason why, in Figure



**Figure 17.** Pareto fronts of the two-objective problem in the case of the design of a low-power SMPS. Comparison between Si only and SiC+Si technologies (Blue and black stars stand for optimal SiC+Si solutions in full-bridge and push-pull topologies, respectively; black circles correspond to Si only solutions in push-pull topology).

18, the conduction losses of the diodes  $P_{D,on}$  ( $\cong 2.8$  W) are practically unchanged from one technology to the other. Still, the use of SiC to implement the freewheeling diode  $D_1$  of the buck stage (the latter operating at twice de switching frequency  $f_s$ ) allows for gain of 52.5% as regards the turn-off losses of the diodes  $P_{D,sw}$ .



**Figure 18.** Power losses distribution in the semiconductor devices of the low-power SMPS. Comparison between Si only and SiC+Si technologies, considering two solutions having the same mass of 100 g.

## 7. Conclusion and perspectives

In this chapter, power losses and mass of optimally designed Si- vs. SiC-based isolated DC-DC power converters have been compared in quantitative terms. Two application examples operating at very different output power levels have been studied: a 100 kW auxiliary railway SMPS and a multiple output 33.5 W SMPS intended for a space application. To that end, a CAD tool dedicated to the MO optimization of isolated DC-DC converters and based on genetic algorithms (NSGA-II in particular) has been employed. Fast analytical models have been used to account for the electrical and thermal phenomena occurring inside the power converters. An important effort has been made to enrich the database of the existing tool with WBG devices (mainly SiC) currently available from manufacturers. The results show clearly that the SiC technology leads to the design of lighter SMPS, with less power losses compared to Si technology only. Besides, the use of the MO optimization CAD tool permits to evaluate the gains in terms of power losses and mass from one technology to the other, which is an advantage.

In future work, the packaging aspects using, e.g., analytical formulas accounting for the component integration in the power converter [40] and electromagnetic compatibility considerations (constraints on the voltage and current gradients) should be included in the tool. Performing a sensitivity analysis could be another perspective. Such an analysis would be useful to give a designer with important information about the stability of one particular optimal solution against others. It should also be reminded that the CAD tool used in this study is a pre-design tool based on simple and fast analytical models. For example, rapid transients on switches and parasitic capacitive effects in the magnetic components are not taken into account. Once the optimal solution is chosen from the tool and the designer know-how, finer models have to be employed around that particular design configuration in order to refine the solution, at the cost of higher computational burden (performing, e.g., transient circuit simulations or using numerical methods such as the FE technique). Lastly, it should be noted that, in this study, GaN-based power transistors were not selected for the space application because their voltage ratings in the database are still too low. Yet since in a near future the commercial offer concerning WBG components is expected to drastically increase, the tool database will be completed over time and, hence, the design possibilities considerably extended.

### Author details

O. Deblecker\*, Z. De Grève and C. Versèle

\*Address all correspondence to: [olivier.deblecker@umons.ac.be](mailto:olivier.deblecker@umons.ac.be)

Electrical Engineering Division, Faculty of Engineering, University of Mons (UMONS), Mons, Belgium

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